UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,170	08/30/2004	Brent A. Anderson	BUR920040040US1	5169

29154 7590 02/07/2006

FREDERICK W. GIBB, III
GIBB INTELLECTUAL PROPERTY LAW FIRM, LLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER	
HO, HOANG QUAN TRAN	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,170	ANDERSON ET AL.	
	Examiner	Art Unit	
	Hoang-Quan Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☒ This action is **FINAL**. 2☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendment dated November 16, 2005 in which claims 1, 5, 10 – 11, 17, 21, and 26 were amended has been entered of record.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Mathew et al. (U.S. Pat. Pub. 2005/0098822).

Regarding claim 1, Fig. 6 of Mathew teaches a field effect transistor (FET) comprising:

a fin structure (14 & 16; Para. 0018);

conducting spacers (42 & 44; Para. 0018) contacting said fin structure, wherein an upper surface of said conducting spacers is substantially planar with an upper

surface of said fin structure (see Fig. 4; approaching edge of 42 & 44 are meet up at the top most fin structure, thus considered planar);

an insulator (66 in Fig. 6) contacting said spacers, wherein said insulator is structurally isolated from said fin structure; and

a gate layer (18; Para. 0021) positioned on said fin structure, said spacers, and said insulator (Fig. 6 shows that 66 is placed on and surrounding the gate layer, therefore the gate layer is also considered on insulator).

Regarding claim 2, Mathew teaches the FET, further comprising:

a substrate (15; Para. 0018); and

an isolation layer (13; Para. 0018) positioned over said substrate (15; Para. 0018),

wherein said isolation layer is positioned under said insulator, said spacers, and said fin structure (see Fig. 6).

Regarding claim 3, Mathew teaches the FET, further comprising source/drain regions above said isolation layer (70 and 72; Para. 0022; see Fig. 5).

Regarding claim 4, Mathew teaches wherein said fin structure comprises an oxide layer (16; Para. 0018) over a silicon layer (14; Para. 0018).

Regarding claim 5, Mathew teaches the FET, further comprising an oxide layer (26; Para. 0019) contacting said fin structure (105).

Regarding claim 6, Fig. 6 of Mathew teaches the FET, further comprising a second oxide layer (28; Para. 0019) over said oxide layer (26), wherein said second oxide layer (28) is planar to said gate layer.

Regarding claims 7 and 8, Mathew teaches the FET, wherein said spacers and said gate layer comprise the same material (Para. 0022; Para. 0036). Mathew discloses that the material can be polysilicon

Regarding claim 9, Mathew teaches the FET, further comprising a gate insulator (26; Para. 0019) positioned between said fin structure and said spacer.

Regarding claim 10, Fig. 5d of Mathew teaches the FET, further comprising a second insulator (13; Para. 0018) contacting said insulator (34).

Regarding claim 11, Fig. 4 of Mathew teaches a field effect transistor (FET) device comprising:

a fin structure (14 & 16; Para. 0018);

a first gate electrode (42; Para. 0018) contacting said fin structure (14 & 16);

a gate insulator (16; Para. 0018) positioned between said first gate electrode (18) and said fin structure (14 & 16);

a second gate electrode (44; Para. 0021) positioned transverse to said first gate electrode (18); and

a third gate electrode (18; Para. 0021) positioned on top of said fin structure (14 & 16), said first gate electrode (42), and said second gate electrode (44).

Regarding claim 12, Fig. 4 of Mathew teaches a FET, further comprising:

a substrate (15; Para. 0018); and

an isolation layer (13; Para. 0018) positioned over said substrate (15),

wherein said isolation layer (13) is positioned beneath said gate insulator (16), said first gate electrode (42), and said fin structure (14 & 16).

Regarding claim 13, Mathew teaches a FET, wherein said isolation layer is isolated from said second gate electrode (Para. 0022). Mathew discloses that sidewall spacers may be formed adjacent to the second gate, therefore a sidewall may be made be in between the second gate and the isolation layer.

Regarding claim 14, Fig. 5 of Mathew teaches a FET, further comprising source/drain regions (70 and 72; Para. 0022) above said isolation layer (13).

Regarding claim 15, Fig. 6 of Mathew teaches a FET, further comprising a dielectric material (66; Para. 0023) sandwiching said second gate electrode (44).

Regarding claim 16, Fig. 6 of Mathew teaches a FET, wherein said fin structure (14 & 16) comprises an oxide layer (16; Para. 0018) over a silicon layer (14; Para. 0018).

Regarding claim 17, Fig. 6 of Mathew teaches a FET, further comprising an oxide layer (26; Para. 0019) contacting said fin structure (14 & 16).

Regarding claim 18, Fig. 6 of Mathew teaches a FET, further comprising a second oxide layer (28; Para. 0019) over said oxide layer (26), wherein said second oxide layer (28) is planar to said third gate electrode (18).

Regarding claims 19 and 20, Mathew teaches a FET, wherein said first gate electrode and said third gate electrode comprise the same material (Para. 0022; Para. 0036). Mathew discloses that the material can be polysilicon.

Regarding claim 21, Fig. 4 of Mathew teaches a method of lowering a gate capacitance and extrinsic resistance in a field effect transistor (FET), said method comprising:

forming a fin structure (14; Para. 0018);

configuring a first gate electrode (42; Para. 0018) contacting said fin structure (14 & 16);

disposing a gate insulator (16; Para. 0018) between said first gate electrode (18) and said fin structure (14 & 16);

positioning a second gate electrode (44; Para. 0021) transverse to said first gate electrode (18); and

depositing a third gate electrode (18; Para. 0021) on top of said fin structure (14 & 16), said first gate electrode (42), and said second gate electrode (44).

Regarding claim 22, Fig. 4 of Mathew teaches a FET, further comprising forming an isolation layer (13; Para. 0018) over a substrate (15; Para. 0018), wherein said isolation layer (13) comprises a buried oxide (BOX) layer (Para. 0018), and wherein said isolation layer (13) is positioned beneath said gate insulator (16), said first gate electrode (42) and said fin structure (14 & 16).

Regarding claim 23, Fig. 5 Mathew teaches a FET, further comprising configuring source/drain regions (70 and 72; Para. 0022) above said isolation layer (13).

Regarding claim 24, Fig. 6 of Mathew teaches a FET, further comprising sandwiching said second gate electrode (44) with a dielectric material (66; Para. 0023).

Regarding claim 25, Fig. 6 of Mathew teaches a FET, wherein said fin structure (14 & 16) is formed by depositing an oxide layer (16; Para. 0018) over a silicon layer (14; Para. 0018).

Regarding claim 26, Fig. 6 of Mathew teaches a FET, further comprising forming an oxide layer (26; Para. 0019) contacting said fin structure (14 & 16).

Regarding claim 27, Fig. 6 of Mathew teaches a FET, further comprising forming a second oxide layer (28; Para. 0019) over said oxide layer (26), wherein said second oxide layer (28) is planar to said third gate electrode (18).

Regarding claims 28 and 29, Mathew teaches a FET, further comprising using the same material to form said first gate electrode and said third gate electrode (Para. 0022; Para. 0036). Mathew discloses that the material can be polysilicon.

Response to Arguments

Applicant's arguments, see page 8, filed 11/16/2005, with respect to claims 1, 5, 10 – 11, 17, 21, and 26 have been fully considered and are persuasive. The objection of claims 1 – 10 regarding the word "adjacent" has been withdrawn.

Applicant's arguments, see pages 8 – 13, filed 11/16/2005, with respect to the rejection(s) of claim(s) 1 – 9 under 102(e) have been fully considered and are

persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Mathew et al. (U.S. Pat. Pub. 2005/0098822).

In regards to the word contacting, Mathew teaches such. Please see claims 11 – 29 explanation below. Mathew overcomes the limitations that previous reference does not teach.

Applicant's arguments, see pages 11 – 12, filed 11/16/2005, with respect to the rejection(s) of claim(s) 1 – 5 and 9 – 10 under 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Mathew et al. (U.S. Pat. Pub. 2005/0098822).

In regards to planar, Mathew teaches such. Fig. 6 shows that they touch at an intersecting point where both objects meet, therefore has some type of planar. Mathew overcomes the limitations that previous reference does not teach.

Applicant's arguments, see pages 12 – 13, filed 11/16/2005, with respect to the rejection(s) of claims 11 – 29 under 102(e) by Mathew (2005/0098822) have been fully considered and are not persuasive. Corrections to the original rejection are made and still stand forth. Reasons for continued rejection set forth below.

In regards to the first gate contacting the fin structure, taking Mathew's Fig. 4 into consideration and comparing with applicant's Figs. 3 and 7, the fin structure as stated

by the applicant, "Collectively, the silicon layer 135 and the oxide layer 125 form the fin structure 170." (Para. 36). However, in applicant's Figs. 3 and 7, it is evident that there are gate dielectrics 160 contacting the fin structure. Mathew's 14 is equivalent to 135 and 16 is equivalent to 125, therefore equivalently comprises the fin structure, and 26 is equivalent to 160. The applicant notes that gate electrode 18 is not contacting the fin structure 14 because the gate insulator 16 is separating 18 from 14. If such a characterization is proper, then the first gate electrode 145 does not contact the fin structure due in part of gate dielectric 160 as seen in applicant's Fig. 3. It was originally claimed that 135 and 125 forms the fin structure as quoted above. Therefore, any claims directing the conducting spacer contacting the fin structure may fail this condition, which could apply to claims 1 – 29.

In regards to the third gate electrode positioned on top of fin structure, first gate electrode and second gate electrode, the Office understands the word "on top" to be "above". So the third gate electrode 18 is above the first and second electrodes 44 and 46.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Quan Ho whose telephone number is (571) 272-8711. The examiner can normally be reached on Monday - Friday, 8AM - 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HQH

January 23, 2006

David Nelms
Supervisory Patent Examiner
Technology Center 2800